Description

ARRAY SUBSTRATE FOR LCD

Technical Field

[1] The present invention relates to an array substrate, a method of manufacturing the array substrate, a liquid crystal display apparatus having the arrays substrate and a method of manufacturing the liquid crystal display apparatus. More particularly, the present invention relates to an array substrate for a strong bonding with a color filter substrate, a method of manufacturing the array substrate, a liquid crystal display apparatus having the arrays substrate and a method of manufacturing the liquid crystal display apparatus.

Background Art

[2] Recently, a liquid crystal display apparatus is widely used, because the liquid crystal display apparatus has lightweight, thin thickness and low power consumption.

[3] The liquid crystal display apparatus includes a liquid crystal display panel and a backlight assembly. The backlight assembly provides light to the liquid crystal display panel. The liquid crystal display panel includes a color filter substrate and an array substrate. The color filter substrate includes color filters through which the light having specific wavelengths may pass to display colored images. The color filter includes a common electrode. A reference voltage is applied to the common electrode.

[4] The array substrate employs a thin film transistor as a switching device. The thin film transistor includes a gate electrode, a drain electrode and a source electrode. The gate electrode is electrically connected to a gate line. The drain electrode is electrically connected to a pixel electrode. The source line is electrically connected to a data line. When a gate voltage is applied to the gate line, the thin film transistor is turned on, so that a pixel voltage is applied to the pixel electrode via the thin film transistor.

[5] A liquid crystal layer is interposed between the color filter substrate and the array substrate. When the pixel voltage is applied to the pixel electrode, electric fields are formed between the pixel electrode and the common electrode. The electric fields change the arrangement of the liquid crystal molecules of the liquid crystal layer to change the transmittance of light provided from the backlight assembly. Therefore, an image is displayed.

[6] According to the conventional liquid crystal display apparatus, the data line does not overlap with the pixel electrode to avoid the increase in power consumption from the cross-talk due to the parasitic capacitance formed between the data line and the

pixel electrode when the data line overlaps with the pixel electrode.

[7] However, when the data line does not overlap with the pixel electrode, the distance between the pixel electrodes increases due to the data line that is disposed between the pixel electrodes. Therefore, aperture ratio is lowered. Furthermore, the light leakage between the data line and the pixel electrode causes lower luminance.

[8] In order to avoid above-mentioned problems, an insulation layer is formed between the data line and the pixel electrode. Therefore, a portion of the data line may overlap with the pixel electrode to increase the aperture ratio.

[9] The insulation layer has a low dielectric constant. Furthermore, when the insulation layer is formed, the distance between the data line and the pixel electrode increases. Therefore, even when a portion of the data line overlaps with the pixel electrode, a parasitic capacitance formed between the data line and the pixel electrode becomes negligibly small. Therefore, the insulation layer formed between the pixel electrode and the data line increases the aperture ratio and prevents the leakage of the light from the backlight assembly.

[10] However, when the insulation layer is formed, the bonding strength between the sealant that combines the color filter substrate and the array substrate, and the insulation layer, or the bonding strength between the insulation layer and the gate insulation layer becomes fragile. Thus, a weak impact may separate the color filter substrate from the array substrate. Even though the color filter substrate is not completely separated from the array substrate, liquid crystal material is not completely injected into between the color filter substrate and the array substrate due to the crack formed between the sealant and the insulation layer or between the insulation layer and the gate insulation layer, which lowers the productivity.

Disclosure of Invention

Technical Problem

[11] The present invention provides an array substrate for a strong bonding with a color filter substrate.

[12] The present invention also provides a method of manufacturing the array substrate.

[13] The present invention also provides a liquid crystal display apparatus having the array substrate.

[14] The present invention also provides a method of manufacturing the liquid crystal display apparatus.

Technical Solution

[15] In accordance with an exemplary array substrate of the present invention, the array substrate includes a transparent substrate, a first insulation layer and a pixel electrode. The transparent substrate includes a display region that displays an image, a peripheral region having a driving circuit for displaying an image through the display region, and a sealine region that surrounds the display region to define the display region and the peripheral region. The first insulation layer is formed over the transparent substrate, and the first insulation layer has an opening window in the sealine region. The pixel electrode is formed on the first insulation layer of the display region.

[16] In accordance with an exemplary liquid crystal display apparatus, the liquid crystal display apparatus includes an array substrate, a color filter substrate, a liquid crystal layer and a sealing member. The array substrate includes a transparent substrate, a first insulation layer, and a pixel electrode. The transparent substrate has a display region that displays an image, a peripheral region having a driving circuit for displaying an image through the display region, and a sealine region that surrounds the display region to define the display region and the peripheral region. The first insulation layer is formed over the transparent substrate, and the first insulation layer has an opening window in the sealine region. The pixel electrode is formed on the first insulation layer of the display region. The color filter substrate faces the array substrate. The liquid crystal layer is interposed between the array substrate and the color filter substrate. The sealing member is formed at the opening window to combine the array substrate and the color filter substrate.

[17] In accordance with an exemplary method of forming an array substrate, a first insulation layer is formed over the transparent substrate including a display region that displays an image, a peripheral region having a driving circuit for displaying an image through the display region, and a sealine region that surrounds the display region to define the display region and the peripheral region. A portion of the first insulation layer is removed to form an opening window in the sealine region. Then, a pixel electrode is formed on the first insulation layer of the display region.

[18] In accordance with an exemplary method of forming a liquid crystal display apparatus, an array substrate including i) a transparent substrate including a display region that displays an image, a peripheral region having a driving circuit for displaying an image through the display region, and a sealine region that surrounds the display region to define the display region and the peripheral region, ii) a first insulation layer formed over the transparent substrate, the first insulation layer having an opening window in the sealine region, and iii) a pixel electrode formed on the first

insulation layer of the display region is formed. A sealing member is formed at the opening window. A color filter substrate is attached to the sealing member to assemble the array substrate and the color filter substrate. Then, a liquid crystal layer is formed between the array substrate and the color filter substrate.

[19] According to the present invention, the bonding of a color filter substrate and an array substrate is reinforced.

[20] Furthermore, a liquid crystal material is completely filled in between the color filter substrate and the array substrate, which increases the productivity.

Brief Description of the Drawings

[21] The above and other advantages of the present invention will become readily apparent by reference to the following detailed description when considered in conjunction with the accompanying drawings wherein:

[22] FIG. 1 is a schematic plan view showing an array substrate;

[23] FIG. 2 is a schematic layout showing an array substrate;

[24] FIGS. 3 and 4 are schematic perspective view showing exemplary opening windows formed on an insulation layer of FIG. 2;

[25] FIG. 5 is a cross-sectional view taken along a line A-A′ of FIG. 2 according to a first exemplary embodiment of the present invention;

[26] FIG. 6 is a cross-sectional view taken along a line A-A′ of FIG. 2 according to a second exemplary embodiment of the present invention;

[27] FIG. 7 is a schematic cross-sectional view showing a liquid crystal display apparatus according to a third exemplary embodiment of the present invention; and

[28] FIGS. 8 to 11 are schematic views showing a process of injecting liquid crystal.

Best Mode for Carrying Out the Invention

[29] FIG. 1 is a schematic plan view showing an array substrate.

[30] Referring to FIG. 1, an array substrate 100 includes a display region DR and a peripheral region PR. The display region DR displays an image, and the peripheral region includes a driving circuit, such as a gate driving circuit 101. A data driving circuit (not shown) is made in the form of separate chip, and the data driving circuit is electrically connected to the array substrate 100. The data driving circuit is also disposed on the peripheral region PR.

[31] A sealine region SLR is disposed between the display region DR and the peripheral region PR, such that the sealine region SLR divides the display region DR and the peripheral region PR. A sealing member (not shown) for bonding the array substrate

and a color filter substrate (not shown) is to be disposed on the sealine region SLR.

[32] The display region DR includes a plurality of gate lines 203 arranged in parallel each other, and a plurality of data lines 102 arranged perpendicular to the gate lines 203. The gate lines 203 and the data lines 102 are formed on different layers and electrically insulated from each other.

[33] Each of the data lines 102 and gate lines 203 defines a pixel. Each pixel includes a thin film transistor 201 and a pixel electrode 103.

[34] The thin film transistor 201 includes a gate electrode G, a source electrode S and a drain electrode D. The gate electrode G is electrically connected to the gate line 203. The source electrode S is electrically connected to the data line 102. The drain electrode is electrically connected to the pixel electrode 103.

[35] When a gate driving circuit (not shown) applies a gate driving voltage to the gate line 203, the thin film transistor 201 that is electrically connected to the gate line 203 is turned on. Then, a pixel voltage that is applied by a data driving circuit (not shown) is applied to the pixel electrode 103 via the thin film transistor 201.

[36] FIG. 2 is a schematic layout showing an array substrate.

[37] Referring to FIG. 2, a plurality of gate lines 203 and a plurality of data lines 102 are formed on different layers of a display region DR of an array substrate 100. A pixel electrode 103 is electrically connected to a thin film transistor 201 via a contact hole 513. A portion of the gate line 203 protrudes to form a gate electrode G of a thin film transistor 201. A gate insulation layer (not shown) is formed on the gate electrode G. An amorphous silicon layer (not shown) and n+ amorphous silicon layer are formed on the gate insulation layer, in sequence. Then, a drain electrode D and a source electrode S are formed on the gate n+ amorphous silicon layer.

[38] A gate driving circuit 101 is formed in a peripheral region PR. A sealine region SLR is interposed between the peripheral region PR and display region DR.

[39] The sealine region SLR includes an opening window 301. A sealant that combines the array substrate 100 and a color filter substrate may be tightly attached to the sealine region SLR by the opening window 301. That is, the bonding strength of the insulation layer (not shown) formed on the array substrate 100 and the sealant is low. Therefore, the insulation layer is removed to form the opening window 301. Then, the sealant is formed on the opening window 301. When the sealant is attached on the opening window 301, a contact area of the sealant increases, and the sealant makes contact with not only the insulation layer but also other layers to strengthen the bonding between the sealant and the array substrate 100.

[40] Therefore, as long as the opening window 301 opens the insulation layer to increase contact area, the shape of the opening window 301 is not limited. As an example, in FIG. 2, the opening window 301 extends in a longitudinal direction of the sealine region SLR. The shape of the opening window 301, however, and the number of the opening window are not limited.

[41] FIGS. 3 and 4 are schematic perspective views showing exemplary opening windows formed on an insulation layer of FIG. 2.

[42] Referring to FIGS. 3 and 4, a portion of an insulation layer 306 is removed to form an opening window 301. The opening window 301 extends in a longitudinal direction of a sealine. The shape, the size and the number of the opening window 301 in FIGS. 3 and 4 do not limit the scope of this invention.

[43] FIG. 5 is a cross-sectional view taken along a line A-A′ of FIG. 2 according to a first exemplary embodiment of the present invention, and FIG. 6 is a cross-sectional view taken along a line A-A′ of FIG. 2 according to a second exemplary embodiment of the present invention.

[44] Referring to FIGS. 5 and 6, array substrates 100a and 100b of FIGS. 5 and 6, respectively, include a first transparent substrate 304, a thin film transistor 201, an insulation layer 306 and a pixel electrode 103.

[45] The first transparent substrate 304 includes a display region DR, a peripheral region PR and a sealine region SLR that divides the display region DR and the peripheral region PR.

[46] The display region DR displays an image, and the peripheral region PR includes driving circuits for displaying an image. A sealant that combines the array substrates 100a and 100b with a color filter substrate is to be disposed in the sealine region SLR.

[47] The display region DR of the first transparent substrate 304 includes a plurality of gate electrode G. A gate insulation layer 305 is formed on the first transparent substrate 304, such that the gate insulation layer 305 covers the gate electrode G. A source electrode S and a drain electrode D are formed over the gate insulation layer D. An insulation layer 306 is formed thereon. The insulation layer 306 includes an opening window 301 and a contact hole 513. The opening window 301 is formed in the sealine region SLR. The contact hole 513 exposes drain electrode D. A pixel electrode 103 formed on the insulation layer 306 is electrically connected to the drain electrode D via the contact hole 513.

[48] Hereinafter, a method of manufacturing the array substrate will be explained.

[49] Aluminum neodymium (Al-Nd) alloy is deposited on the first transparent substrate

304 to form a layer. The layer comprising aluminum neodymium (Al-Nd) alloy is patterned via photolithography process and etched to form a gate electrode G.

[50] When the gate electrode G is formed, a gate insulation layer (or a second insulation layer) 305 is formed, such that the gate insulation layer covers the gate electrode G. The gate insulation layer comprises silicon nitride (SiNx).

[51] An amorphous silicon layer 302 is formed on a portion of the gate insulation layer 305, which is near the gate electrode G.

[52] An n+ amorphous silicon layer 303 is formed on the amorphous silicon layer 302.

[53] The gate insulation layer 305 has a high resistivity at a low temperature, so that the carriers of the amorphous silicon layer, when a voltage is applied to the gate electrode, do not leak but gather together at an interface between the amorphous silicon layer 302 and n+ amorphous silicon layer 303 to form a channel layer.

[54] The amorphous silicon layer 302 has a resistivity ranged from about $10^{11}\Omega cm^{-1}$ to about $10^{12}\Omega cm^{-1}$. When a gate voltage is applied to the gate electrode G, the resistivity of the amorphous silicon layer 302 is lowered to be $10^{5}\Omega cm^{-1}$ to about $10^{6}\Omega cm^{-1}$. Therefore, current may pass through the amorphous silicon layer.

[55] The n+ amorphous silicon layer 303 reduces a contact resistance between a metal of the source electrode S and the drain electrode D, and the amorphous silicon layer 302, and the n+ amorphous silicon layer 303 reduces leakage current. Phosphorus (P) atoms are doped to form the n+ amorphous silicon layer 303.

[56] Then, the drain and source electrodes D and S are formed on the n+ amorphous silicon layer 303. The drain and source electrodes D and S comprise chromium.

[57] A gate driving circuit 101 is formed in the peripheral region PR of the first transparent substrate 304. A data driving circuit (not shown) may be made in the form of separate chip, and the chip is disposed in the peripheral region PR.

[58] After the drain and source electrodes D and S are formed, an insulation layer (or a first insulation layer 306) is formed. The insulation layer 306 increases an aperture ratio and luminance. The insulation layer 306 includes a material capable of photolithography process.

[59] The opening window 301 is formed in the sealine region SLR, and the opening window 301 penetrates the insulation layer 306. The opening window 301 may penetrate only the insulation layer 306 to expose the gate insulation layer 305 as shown in FIG. 5, or the opening window 306 may penetrate both the insulation layer 306 and the gate insulation layer 305 to expose the first transparent substrate 304 as shown in FIG. 5.

[60] The opening window 301 may be formed by dry etching. When the opening window 301 is formed, a sealant (not shown) is attached on the array substrates 100a and 100b more tightly.

[61] A contact hole 513 for exposing the drain electrode is formed at the insulation layer 306. The contact hole 513 and the opening window 301 may be formed via a same process or different process.

[62] A layer comprising an optically transparent and electrically conductive material, for example, such as indium tin oxide (ITO), indium zinc oxide (IZO), etc. is formed on the insulation layer 306, and the layer is patterned to form the pixel electrode 103.

[63] The indium tin oxide and the indium zinc oxide have excellent conductivity and are also chemically and thermally stable.

[64] FIG. 7 is a schematic cross-sectional view showing a liquid crystal display apparatus according to a third exemplary embodiment of the present invention.

[65] Referring to FIG. 7, a liquid crystal display apparatus according to a third exemplary embodiment of the present invention includes a color filter substrate 401, an array substrate 100 and a liquid crystal layer 402 interposed between the color filter substrate 401 and the array substrate 100.

[66] The color filter substrate 401 includes a second transparent substrate 407, a color filter 405, a leveling layer 404, a common electrode 403 and a black matrix 406.

[67] The black matrix 406 and the color filter 405 are formed on the second transparent substrate 407. The leveling layer 404 covers the black matrix 406 and the color filter 405. The common electrode 403 is formed on the leveling layer 404.

[68] The color filter 405 includes a red color filter R, a green color filter G and a blue color filter B. When a light passes through the red, green and blue color filters R, G and B, the light is filtered to display a red, green and blue light, respectively.

[69] A liquid crystal display apparatus is classified into stripe type, mosaic type, a triangular type, etc in accordance with an arrangement of the red, green and blue color filters. The stripe type is adequate for a monitor of a computer system, and the mosaic type and the triangular type are adequate for a television set.

[70] The black matrix 406 covers the driving circuit formed on the array substrate to prevent the driving circuit, etc. from being seen. The black matrix 406 comprises metal or organic material.

[71] The leveling layer 404 protects the color filter 405, and increases the flatness by decreasing the height differences. The leveling layer 404 comprises acryl resin or polyimide resin.

[72] The common electrode 403 comprises a material that is optically transparent and electrically conductive, for example, such as indium tin oxide (ITO), indium zinc oxide (IZO), etc.

[73] Hereinafter, a method of forming the color filter substrate 401 will be explained.

[74] The black matrix 406 is formed on the second transparent substrate 407. The black matrix 406 comprises metal or organic material.

[75] A metal black matrix is classified into chromium (Cr) black matrix, a double-layered chromium black matrix (Cr/CrOx) or a triple-layered chromium black matrix (Cr/CrNx/CrOx). An organic black matrix is divided into a carbon black type black matrix, an RGB pigment black matrix, a dye dispersion type black matrix, and an RGB overlapping type black matrix.

[76] The color filter 405 is formed on the second transparent substrate 407. The color filter 405 includes a red color filter R, a green color filter G and a blue color filter B. The color filter 405 may be formed using dyes or pigments. A method of forming the color filter 405 using dyes is classified into a dyeing process and a dye dispersion process, and a method of forming the color filter 405 using pigments is classified into a pigment dispersion process, a printing process and an adhesion process.

[77] In the dyeing process, acryl resin, casein, gelatin, etc are used as a coloring resin, and dye is used as a coloring matter. The dyeing process is adequate for a minute opening window, but the color filter 405 formed by the dyeing process has a low durability.

[78] In the dye dispersion process, polyimide is used as the coloring resin, and dye is used as the coloring matter. The dye dispersion process is also adequate for a minute opening window, but the color filter 405 formed by the dye dispersion process has a low durability.

[79] In the pigment dispersion process, acryl resin is used as the coloring resin, and pigments are used as the coloring matter. The color filters 405 formed by the pigment dispersion process have a good lightproof property and a good thermal stability. However, oxygen preventing layer is required additionally.

[80] In the printing process, epoxy resin is used as the coloring resin, and the pigments are used as the coloring matter. The color filters 405 formed by the printing process have a good lightproof property and a good thermal stability, but a bad resolution and flatness.

[81] In the adhesion process, both the acryl resin and the epoxy resin are used as the coloring resin, and the pigments are used as the coloring matter. The color filters 405

formed by the adhesion process have a good lightproof property, a flatness and a good thermal stability, but the patterning is limited.

[82] The dyeing process, the dye dispersion process and the pigment dispersion process are adequate for the stripe, mosaic and triangular type arrangements of the color filters. The printing process and the adhesion process are adequate for the stripe arrangement, but not for the mosaic, and triangular type arrangements.

[83] The leveling layer 404 is formed on the black matrix 406 and the color filter 405. The leveling layer 404 comprises acryl resin or polyimide resin.

[84] When the acryl resin is used for the leveling layer 404, the acryl resin is mixed with a hardener to form the leveling layer 404. The polyimide resin is costing much, but the polyimide resin has a good thermal stability.

[85] When the leveling layer 404 is formed, a hardening process is performed.

[86] Both the acryl resin and the polyimide resin are thermosetting plastic. Therefore, heat treatment is important. Additionally, when the hardening process is defectively performed, the common electrode 403 that is to be formed on the leveling layer 404 may be corrugated or fragile. Therefore, the leveling layer 404 is sufficiently hardened.

[87] The common electrode 403 is formed on the leveling layer 404. The common electrode 403 comprises a material that is optically transparent and electrically conductive, for example, such as indium tin oxide (ITO), indium zinc oxide (IZO), etc.

[88] Hereinbefore, a method of forming the color filter substrate 401 was explained. A method of forming the array substrate 100 was explained already.

[89] The color filter substrate 401 and the array substrate 100 are bonded together by the sealant (408). The sealant 408 is formed along the sealine region SLR of FIG. 1, such that the sealant 408 surrounds the display region DR. A small portion of the sealant 408, however, is opened.

[90] The sealant 408 makes contact with the gate insulation layer 305 or the first transparent substrate 304 via the opening window 301 formed at the insulation layer 306.

[91] A spacer 514 maintains a distance between the array substrate 100 and the color filter substrate 401 that is bonded by the sealant 408. The spacer 514 is disposed over the contact hole 513. The black matrix 406 covers the spacer 514 to prevent the spacer 514 from being seen outside.

[92] When the color filter substrate 401 are assembled with the array substrate 100, liquid crystal is injected into between the color filter substrate 401 and the array substrate 100 to form a liquid crystal layer.

[93] FIGS. 8 to 11 are schematic views showing a process of injecting liquid crystal.

[94] Referring to FIG. 8, a bonded module 601 of the color filter substrate 401 and the array substrate 100 is loaded in a chamber 600.

[95] Then, a pressure of the chamber 600 is lowered to be about $5x10^{-3}$Torr.

[96] Referring to FIG. 9, the chamber 600 is closed, and the bonded module 601 of the color filter substrate 401 and the array substrate 100 is dipped into the liquid crystal material 602. A pressure of the space between the color filter substrate 401 and the array substrate 100 is same as the pressure of the chamber. Thus, the liquid crystal material is not injected into between the space between the color filter substrate 401 and the array substrate 100.

[97] Referring to FIGS. 10 and 11, the chamber 600 is opened and the inert gas is injected into the chamber to raise the pressure of the chamber. Then, the pressure of the chamber is higher than the pressure of the space between the color filter substrate 401 and the array substrate 100. Therefore, the liquid crystal material 602 is injected into between the color filter substrate 401 and the array substrate 100.

[98] According to a conventional liquid crystal display apparatus, cracks are formed between the sealant 408 and the insulation layer 306 or between the insulation layer 306 and the gate insulation layer 305. Therefore, the liquid crystal material is not injected into between the color filter substrate 401 and the array substrate 100 due to poor vacuum in bonded module 601.

[99] However, according to the present invention, the bonding of the sealant 408 and the insulation layer 306 is reinforced to prevent the cracks between the sealant and the insulation layer. Therefore, the liquid crystal material 602 is completely filled.

Industrial Applicability

[100] According to the present invention, a bonding of a color filter substrate and an array substrate is reinforced.

[101] Furthermore, liquid crystal material is completely filled in between the color filter substrate and the array substrate.

[102] Although the exemplary embodiments of the present invention have been described, it is understood that the present invention should not be limited to these exemplary embodiments but various changes and modifications can be made by one ordinary skilled in the art within the spirit and scope of the present invention as hereinafter claimed.